IN THE SPECIFICATION:

Please amend paragraph **[0004]** as follows:

[0004] While it is generally preferred to harden the gate oxides of P-channel devices due to the nature of P-type dopants, such is not the case for N-channel devices. Hardening of ~~N-channel~~ N-channel devices is generally not necessary as N-type dopants do not readily diffuse through ~~non-hardened~~ non-hardened gate oxides. Moreover, hardening N-channel devices is often undesirable due to compounding performance problems. As is well known, hardening of gate oxides included in ~~N-channel~~ N-channel devices leads to significant threshold voltage (V_T) roll-off. While V_T roll-off can be counteracted through enhancement implants, the increased dopant concentration resulting from enhancement implants causes additional performance problems, such as refresh degradation and reduced surface mobility. Therefore, it would generally be advantageous not to harden the gate oxides of N-channel devices included within an IC device.

Please amend paragraph **[0005]** as follows:

[0005] Despite the difficulties generally resulting from hardening the gate oxides of ~~N-channel~~ N-channel devices, however, the ability to selectively harden the gate oxides of N-channel devices in particular instances would be advantageous.

Please amend paragraph **[0013]** as follows:

[0013] As can be easily appreciated by one of skill in the art, the present invention enables fabrication of an IC device including N-channel and P-channel devices having hardened or non-hardened gate oxides of varying thicknesses ~~without the need of the etch steps~~ made necessary by known methods. Moreover, the method of the present invention may be easily integrated into known fabrication processes using known technology, and, because the method of the present invention does not require etching of the gate oxide layer to achieve gate oxides of varying thicknesses, the method of the present invention is cost effective and will continue to be useful as device dimensions shrink beyond the dimensions of those devices currently considered to be state of the art.

Please amend paragraph **[0018]** as follows:

[0018] RPN treatments are well known in the art, and in the context of this invention, either a true RPN treatment or an HDP RPN treatment may be used. Generally, the process parameters of the RPN treatment used to harden the exposed area 20 of the gate oxide layer may be varied to produce desired results in various fabrication contexts. However, the temperature of the RPN treatment must be low enough that the patterned first resist layer 16 remains stable through the entire process. For example, it is presently preferred to use an HDP RPN conducted for approximately 1 second to approximately 30 seconds at about ~~30° C~~ 30°C to about ~~90° C~~ 90°C using about 800 watts to 3000 watts of power. Such a method effectively hardens the exposed area 20 of the gate oxide layer 14, yet runs at a temperature well below that which might render the resist unstable.

Please amend paragraph **[0019]** as follows:

[0019] As can be seen in drawing FIG. 4, following the first RPN treatment 22, the remaining portions of the first resist layer 16 are removed, resulting in a first intermediate structure 24. The first intermediate structure 24 includes the semiconductor substrate 10 with a partially hardened gate oxide layer 26, which may be used as desired in the fabrication of ~~N-channel~~ N-channel or P-channel devices. Generally, the non-hardened portion 28 of the partially hardened gate oxide layer 26 will be used to fabricate at least one N-channel device, while the hardened portion 30 of the partially hardened gate oxide layer 26 will be used to fabricate at least one ~~P-channel~~ P-channel device. As will be appreciated by one of skill in the art, various methods for fabricating both N-channel and P-channel devices are well known, and after selectively hardening the gate oxide layer, the method of the present invention may include any suitable fabrication process necessary to complete fabrication of a desired IC device.

Please amend paragraph **[0021]** as follows:

[0021] As was true with the partially hardened gate oxide layer 26 of the first intermediate structure 24 formed by the first embodiment of the method of the present invention,

the second partially hardened gate oxide layer 32 may be used as desired to form gate oxides for N-channel or P-channel devices. For example, the thick, non-hardened portion 34 of the second partially hardened gate oxide layer 32 may be used to form a gate oxide for one or more ~~N-channel~~ N-channel devices, while the hardened portion 30 of the second partially hardened gate oxide layer 32 may be used to form a gate oxide for one or more P-channel devices. Again, various methods for fabricating an IC device including N-channel and P-channel devices using an intermediate structure, such as the second intermediate structure 31 illustrated in drawing FIG. 6, are well known, and the method of the present invention may include any such suitable method.

Please amend paragraph **[0025]** as follows:

[0025] Of course, it should be understood that the three embodiments of the method of the present invention discussed herein are provided for illustrative purposes only. The method of the present invention is easily varied to provide IC devices having any desired combinations of hardened or non-hardened gate oxides of varying thicknesses. For example, the first resist layer used in the first and second embodiments of the method of the present invention may be patterned such that, following the RPN process, multiple hardened or non-hardened portions are formed within the gate oxide layer. Additionally, where multiple non-hardened portions are formed within the gate oxide layer, the intermediate structure may be processed according to the second embodiment of the method of the present invention to produce a partially hardened gate oxide layer including one or more hardened portions as well as multiple thick, non-hardened portions, which may be used in fabricating thick gate oxides for N-channel devices. Finally, use of additional masking, growth, and RPN steps can produce virtually any number of different hardened areas of varying thicknesses within a single gate oxide layer. Such a gate oxide layer can be used to form an IC device having any desired combination of selectively hardened ~~N-channel~~ N-channel or P-channel devices having gate oxides of different thicknesses.